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EXAMINER	
JAMAL, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2643	6

DATE MAILED: 01/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,689	BEUTLER ET AL.	
	Examiner	Art Unit	
	Alexander Jamal	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-7** rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (5870046), and further in view of Staffiere (6137671).

a. **Claim 1:** Scott discloses a high voltage isolation barrier structure (Abstract) comprising:

i. First and second electrodes (Capacitor 209 Fig. 2).

However, Scott does not disclose forming the capacitor by disposing the first electrode on a first side of a circuit board substrate and the second electrode on the second side of the substrate so that the substrate between the electrodes acts as a dielectric material for the capacitive structure.

Staffiere discloses that the creation of a capacitor embedded within a printed circuit board can allow the designer to reduce the required size (and therefore the cost) of the circuit board and any assembly for which the board may be placed in (Col 1 lines 21-30). He further discloses a capacitive structure (Fig. 15) comprising electrode 640 disposed on the first side of the substrate 650, and electrode 660 disposed on a second side of the substrate. The Substrate functions as a dielectric between the electrodes (Col 7 lines 48-64). He further discloses that the electrodes may be embedded within or on the

surface (of either side) of the substrate (Col 8 lines 17-25). It would have been obvious to one of ordinary skill in the art at the time of this application to implement the isolation barrier capacitors within the printed circuit board for the purpose of reducing the required circuit board surface area (which may also reduce the size and cost of the circuit).

b. **Claim 2:** In Scott's high voltage isolation barrier, capacitor 209 (Fig. 2) has system side circuitry 225 coupled to the first electrode and line side circuitry 226 coupled to the second electrode (Col 8 lines 29-43).

c. **Claim 3:** Scott discloses a data access arrangement (Scott: Col 8 lines 29-43) comprising isolation capacitor 209 implemented on the circuit board taught by Staffiere.

d. **Claims 4/5:** Scott discloses a data access arrangement comprising isolation capacitor 209 implemented on the circuit board taught by Staffiere and contained within a modem (Col 1 lines 36-47). A modem is inherently used in a computer system for the purpose of having the computer system interacting with and providing/retrieving data to/from the modem.

e. **Claim 6:** With Scott's isolation capacitors implemented on a circuit board as taught by Staffiere, the circuit board will comprise radio frequency circuitry (Scott: Col 11 lines 40-57). The 100pF value of the capacitors are radio frequency circuitry, as well as the processing circuitry in system side circuitry 225 and line side circuitry 226 (Scott: Fig. 2).

f. **Claim 7:** Staffiere discloses a multi-layer circuit board (Fig. 15: Col 7 lines 48-64) with a plurality of substrates (comprising materials 620,650 in Fig. 15).

3. **Claims 8-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (5870046), and further in view of Staffiere (6137671).

a. **Claim 8:** Scott discloses a data access arrangement (Abstract) comprising:

i. First and second electrodes (Capacitor 209 Fig. 2)

ii. Capacitor 209 (Fig. 2) has system side circuitry 225 coupled to the first electrode and line side circuitry 226 coupled to the second electrode (Col 8 lines 29-43).

However, Scott does not disclose forming the capacitor by disposing the first electrode on a first side of a circuit board substrate and the second electrode on the second side of the substrate so that the substrate between the electrodes acts as a dielectric material for the capacitive structure.

Staffiere discloses that the creation of a capacitor embedded within a printed circuit board can allow the designer to reduce the required size (and therefore the cost) of the circuit board and any assembly for which the board may be placed in (Col 1 lines 21-30). He further discloses a capacitive structure (Fig. 15) comprising electrode 640 disposed on the first side of the substrate 650, and electrode 660 disposed on a second side of the substrate. The Substrate functions as a dielectric between the electrodes (Col 7 lines 48-64). He further discloses that the electrodes may be embedded within or on the surface (of either side) of the substrate (Col 8 lines 17-25). It would have been obvious to one of ordinary skill in the art at the time of this application to implement the isolation

barrier capacitors within the printed circuit board for the purpose of reducing the required circuit board surface area (which may also reduce the size and cost of the circuit).

b. **Claim 9:** In Scott's data access arrangements (in Figs. 2 and 7), the system side circuitry can communicate with the host system and the line side circuitry can communicate over a telephone network as described in (Fig. 1: Col 6 line 56 to Col 7 line 20).

c. **Claim 10:** In Scott's data access arrangement, capacitor 209 (Fig. 2) provides high voltage isolation between the system and line side circuitry (Col 7 lines 60-64).

d. **Claim 11:** In Staffiere's circuit board, the electrodes of the embedded capacitor are substantially overlapping (Fig 15: Col 7 lines 47-64).

e. **Claim 12:** A portion of Scott's system side circuitry (comprising the coupling means from one electrode of the isolation capacitor to the rest of the circuitry) is part of the electrode/heat sink 660 (Staffiere: Fig. 15 Col 7 lines 48-64). The portion of Scott's line side circuitry comprises the coupling means from the other electrode 640 of the isolation capacitor to the rest of the line side circuitry. These two portions implemented on the circuit board taught by Staffiere are formed on opposite sides of substrate 650 (Staffiere: Fig. 15).

f. **Claim 13:** Staffiere discloses that the electrical conductor (which forms the first and second electrodes in Fig. 15) can be made from copper (Col 6 lines 11-14).

g. **Claim 14:** In Scott's data access arrangement, the data and control information (clock signal) are communicated between the system and line side circuits in a serialized digital format via the capacitor (Col 4 lines 30-44).

h. **Claim 15:** In Scott's data access arrangement, there is one additional capacitor 210 (Scott: Fig. 2) coupled between system side circuitry 225 and line side circuitry 226.

Although Staffiere does not specify a circuit board with two embedded capacitors in Fig. 15, he states that many permutations of the arrangement can be adapted for specific applications (Staffiere: Col 7 lines 61-64), this would include the DAA disclosed by Scott. Staffiere further discloses another embodiment in Fig. 13b, with a first and second capacitor formed with the substrate between each set of electrodes (Staffiere: Col 6 line 59 to Col 7 line 14).

i. **Claim 16:** Staffiere discloses a multi-layer circuit board (Fig. 15: Col 7 lines 48-64) with a plurality of substrates (comprising materials 620,650 in Fig. 15).

j. **Claim 17:** In Staffiere's circuit board (Fig. 15), the first electrode 640 and 670B is formed on multiple substrates (on either side of substrate 710).

k. **Claim 18:** Staffiere discloses that the electrodes (conducting layers) are printed on the substrate by a screening process (Col 6 lines 20-35).

4. **Claims 19-28** rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (5870046), and further in view of Staffiere (6137671).

a. **Claim 19:** Scott discloses method of manufacturing a communications device (Abstract) comprising:

i. Using the first and second electrodes (Capacitor 209 Fig. 2)

ii. Coupling one electrode of Capacitor 209 (Fig. 2) to first communications circuitry (the first communications circuitry comprising the coupling means from one electrode of the isolation capacitor to the rest of the system side circuitry 225) and the second electrode coupled to second communications circuitry (The second communications circuitry comprises the coupling means from the other electrode of the isolation capacitor to the rest of the line side circuitry 226) (Col 8 lines 29-43).

However, Scott does not disclose forming the capacitor by disposing the first electrode on a first side of a circuit board substrate and the second electrode on the second side of the substrate so that the substrate between the electrodes acts as a dielectric material for the capacitive structure.

Staffiere discloses that the creation of a capacitor embedded within a printed circuit board can allow the designer to reduce the required size (and therefore the cost) of the circuit board and any assembly for which the board may be placed in (Col 1 lines 21-30). He further discloses a capacitive structure (Fig. 15) comprising electrode 640 disposed on the first side of the substrate 650, and electrode 660 disposed on a second side of the substrate. The Substrate functions as a dielectric between the electrodes (Col

7 lines 48-64). He further discloses that the electrodes may be embedded within or on the surface (of either side) of the substrate (Col 8 lines 17-25). It would have been obvious to one of ordinary skill in the art at the time of this application to implement the isolation barrier capacitors within the printed circuit board as part of Scott's method, for the purpose of reducing the required circuit board surface area (which may also reduce the size and cost of the circuit).

b. **Claim 20:** In Scott's method, the first and second communication circuits (as described in the rejection of Claim 19), along with the isolation capacitors form a portion of a data access arrangement (ABSTRACT).

c. **Claim 21:** In Scott's data access arrangement, capacitor 209 (Fig. 2) provides high voltage isolation between the system and line side circuitry (Col 7 lines 60-64).

d. **Claim 22:** In Staffiere's circuit board, the electrodes of the embedded capacitor are substantially overlapping (Fig 15: Col 7 lines 47-64).

e. **Claim 23:** Staffiere discloses a multi-layer circuit board (Fig. 15: Col 7 lines 48-64) with a plurality of substrates (comprising materials 620,650 in Fig. 15).

f. **Claim 24:** In Staffiere's circuit board (Fig. 15), the first electrode 640 and 670B is formed on multiple substrates (on either side of substrate 710).

g. **Claim 25:** Scott's first communications circuitry (comprising the coupling means from one electrode of the isolation capacitor to the rest of the circuitry) is part of the electrode/heat sink 660 (Staffiere: Fig. 15 Col 7 lines 48-64). Scott's second communications circuit comprises the coupling means from the other electrode 640

(Staffiere: Fig. 15 Col 7 lines 48-64) of the isolation capacitor to the rest of the line side circuitry. These two portions implemented on the circuit board taught by Staffiere are formed on opposite sides of substrate 650 (Staffiere: Fig. 15).

h. **Claim 26:** Staffiere discloses that the electrical conductor (which forms the first and second electrodes in Fig. 15) can be made from copper (Col 6 lines 11-14).

i. **Claim 27:** Staffiere discloses that the electrodes (conducting layers) are printed on the substrate by a screening process (Col 6 lines 20-35).

j. **Claim 28:** In Scott's data access arrangement, the data and control information (clock signal) are communicated between the first and second communication circuits via the capacitor formed within the circuit board (Col 4 lines 30-44).

5. **Claims 29-31** rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (5870046), and further in view of Staffiere (6137671).

a. **Claim 29:** Scott discloses a data access arrangement for a modem (Abstract, Col 1 lines 36-47) comprising:

i. A modem is inherently used in a computer system for the purpose of having the computer system interacting with and providing/retrieving data to/from the modem.

ii. A computer system inherently comprises a data bus for the purpose of transporting data to various locations within the computer system.

iii. A computer system inherently comprises a processor coupled to the data bus for the purpose of managing and processing the data being transported on the data bus.

iv. The modem is inherently coupled to the data bus of the computer for the purpose of transmitting/receiving data to/from the processor and rest of the computer system.

v. Capacitor 209 (Fig. 2) with two electrodes.

vi. Capacitor 209 (Fig. 2) has system side circuitry 225 coupled to the first electrode and line side circuitry 226 coupled to the second electrode (Col 8 lines 29-43).

vii. In Scott's data access arrangements (in Figs. 2 and 7), the system side circuitry can communicate with the host system and the line side circuitry can communicate over a telephone network as described in (Fig. 1: Col 6 line 56 to Col 7 line 20).

However, Scott does not disclose forming the capacitor by disposing the first electrode on a first side of a circuit board substrate and the second electrode on the second side of the substrate so that the substrate between the electrodes acts as a dielectric material for the capacitive structure.

Staffiere discloses that the creation of a capacitor embedded within a printed circuit board can allow the designer to reduce the required size (and therefore the cost) of the circuit board and any assembly for which the board may be placed in (Col 1 lines 21-

30). He further discloses a capacitive structure (Fig. 15) comprising electrode 640 disposed on the first side of the substrate 650, and electrode 660 disposed on a second side of the substrate 650. The Substrate functions as a dielectric between the electrodes (Col 7 lines 48-64). He further discloses that the electrodes may be embedded within or on the surface (of either side) of the substrate (Col 8 lines 17-25). It would have been obvious to one of ordinary skill in the art at the time of this application to implement the isolation barrier capacitors within the printed circuit board as part of Scott's method, for the purpose of reducing the required circuit board surface area (which may also reduce the size and cost of the circuit).

b. **Claim 30:** In Scott's data access arrangement, capacitor 209 (Fig. 2) provides high voltage isolation between the system and line side circuitry (Col 7 lines 60-64).

c. **Claim 31:** Staffiere discloses a multi-layer circuit board (Fig. 15: Col 7 lines 48-64) with a plurality of substrates (comprising materials 620,650 in Fig. 15). In Staffiere's circuit board (Fig. 15), the first electrode 640 and 670B is formed on multiple substrates (on either side of substrate 710).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 703-305-3433. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 703-305-4708. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9315 for After Final communications.

DUC NGUYEN
PRIMARY EXAMINER

AJ
January 5, 2004